W-BAND COLLISION AVOIDANCE RADAR FOR LIGHT RAIL APPLICATIONS

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ABSTRACT

W-Band Radar Transceiver System is applied to the application of detecting obstacles on the direct Rail path of an on-coming train. This paper presents the system concept, and the initial data confirming the performance requirement of detecting an adult 1000 ft away in a highly cluttered environment. This work was performed on contract for the Siemens Transportation Systems, Inc. and Los Angeles County Metropolitan Transportation Authority.

INTRODUCTION

The TRW RailSentry Transceiver consists of transmitter and a Receiver, both operating at the radiated frequency range from 94.0 to 94.5 GHz. A common sweeping 4.0 to 4.5 GHz Yttrium Iron Garnet (YIG) oscillator signal source is applied to the Transmitter and to the Receiver, thereby enabling the Digital Signal Processor (DSP) to extract only the desired reflected signal from all other reflections. The DSP converts the output analog signal to the digital equivalent through a Fast Fourier Transform (FFT). Through software, the Radar is able to distinguish the desired target from all other stationary reflections. The DSP portions of the Radar Systems are not addressed here. This paper is directed at the RF transceiver.The isometric and top views of the Transceiver are presented in Figures 1 and 2.

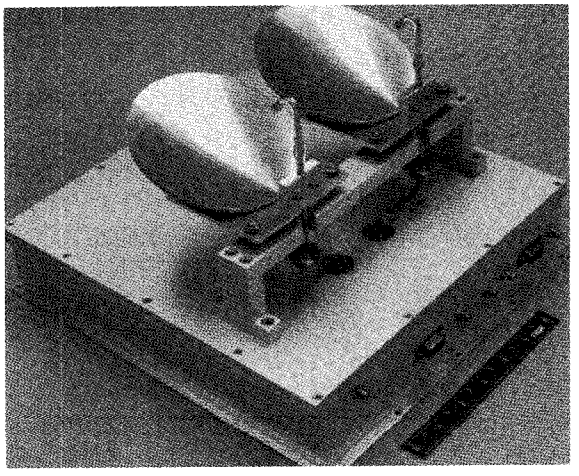

Fig. 1. Isometeric view of Radar Transceiver.

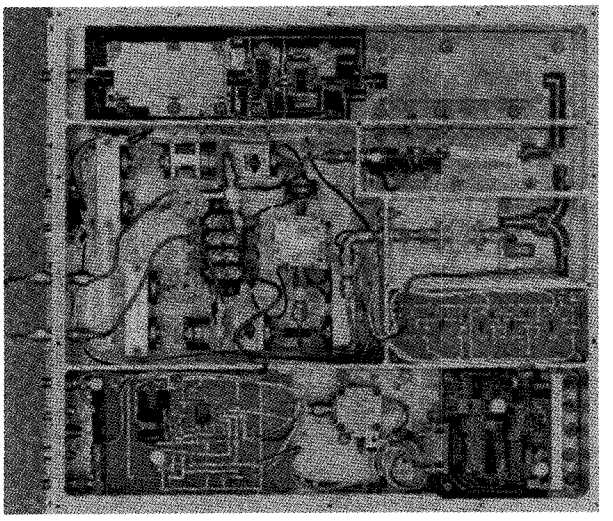

Fig. 2. Top view of RadarTransceiver with top cover removed.

TRANSCEIVER DESCRIPTION

TRANSMITTER

The Transmitter portion of the Transceiver relies on a Dielectric Resonator Oscillator (DRO) operating at 22.50 GHz. The RF signal is multiplied to 90.0 GHz. The 90.0 GHz signal is applied to the Transmitter and also to the Receiver. Both DRO and YIG signals are mixed up to the frequency range from 94.0 to 94.50 GHz. The upconverted frequency signal is amplified and transmitted. The 90 GHz signal is also applied to the Receiver. The times four frequency multiplier, mixer, and power amplifier are MMIC designs. The devices utilized in these circuits were developed in-house. In addition, the isolators are required to isolate the transmitted signals form the received signal were also in-house invented due to the combination of operating frequency and size.

There are two types of antennas used in this system; a low gain pair of horn antennas, and a pair of high gain parbolic section antennas. One antenna is used to transmit and the other to receive. The antennas are used in matched pairs, depending on the topography of the particular location in which each Transceiver is placed. The Transceiver Block Diagram is presented in Figure 3.

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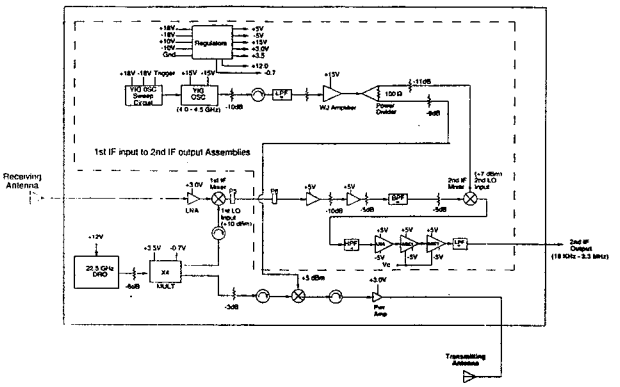


Fig. 3. Transceiver Block Diagram.

W-BAND FREQUENCY SOURCE

The W-Band source is a delectric resonator stabilized oscillator with an output frequency of 22.5 GHz. The signal from the 22.5 GHz source is multiplied to 90 GHz by a X4 MMIC multiplier chip, and amplified to +13.4 dBm by two cascaded MMIC power amplifier stages. The DRO/X4 housing material is A-40. A photograph of the multiplier assembly is shown in Figure 4.

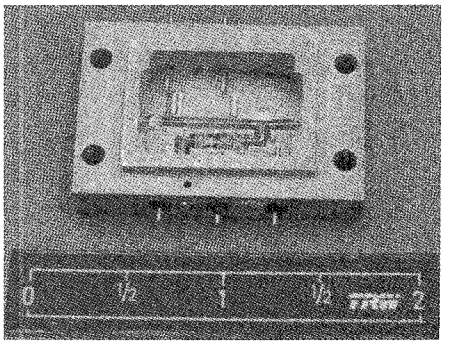


Fig. 4. Photograph of multiplier assembly.

MMIC POWER AMPLIFIER

The power amplifier is a MMIC based design that uses three amplifiers cascaded in series to generate 18.0 to 18.3 dBm output power at 94 GHz. The first chip is the ALT101CA low noise amplifier chip which is a gain stage and has typically 12 to 14 dB gain. The second chip is the APH117C predriver which has 6 dB gain and drives the APH118C output power amplifer. A photograph of the ampilifier assembly is shown in Figure 5. The MMIC chips and substrates are attached to the floor of the housing with conductive epoxy.The amplifier is environmentally sealed with solder-in feedthroughs, and epoxy attached windows and top cover. The housing is A-40 material. The transmitter produces an output power of +18 dBm. In Figure 6 is shown a plot of the output power versus input power for the APH118C MMIC power amplifier chip. Additional data is presented in Table 1.

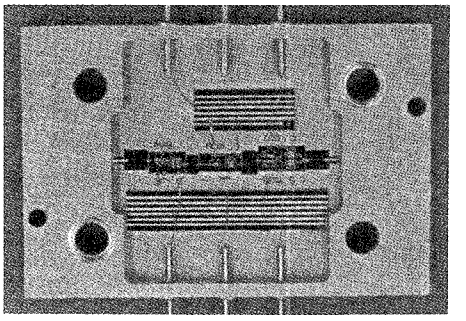


Fig. 5. MMIC power amplifier circuit assembly.

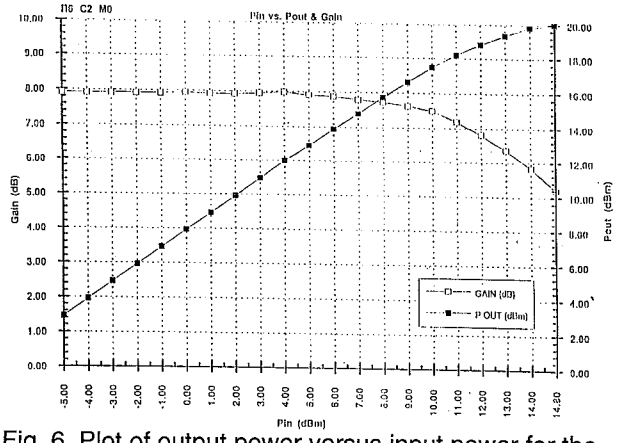


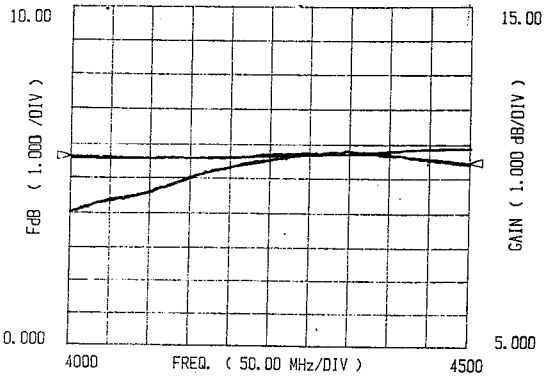
Fig. 6. Plot of output power versus input power for the APH118C MMIC amplifier chip.

P INPUT (DBM)	FREQ (GHZ)						
	93.9	94.0	94.1	94.2	94.3	94.4	94.5
0	18.32	18.10	17.94	18.07	18.29	18.34	18.17
1	18.35	18.13	17.97	18.10	18.33	18.38	18.22
2	18.38	18.16	18.00	18.13	18.35	18.41	18.25
3	18.39	18.17	18.02	18.15	18.37	18.43	18.27
4	18.41	18.19	18.04	18.16	18.39	18.45	18.29
5	18.41	18.20	18.04	18.17	18.40	18.46	18.30

Table 1. Transmitter ouput power is 62 to 70 milliwatts.

RECEIVER

The Receiver portion of the Transceiver consists of a Low Noise Amplifier (LNA), a mixer, and additional hardware operating at lower frequencies.The Receiver LNA noise figure measurement of 5.0 dB is presented in Figure 7. The Receiver front end (LNA and first mixer) noise figure is 5.7 dB.



7. Receiver noise figure and gain.

MMIC LOW NOISE FRONTEND AMPLIFIER

The LNA is a MMIC based design using a single PHEMT chip. This chip is a 3-stage design with 2 single ended stages driving a balanced output stage. Typical performance is 4.8 to 5.0 dB noise figure with 20.4 to 21.1 dB gain from 93.8 to 94.8 GHz. The amplifier uses fused silica substrates with chrome/gold metallization and E-plane Waveguide transitions. The substrates and MMIC are direcly attached to the floor of the IMA with conductive epoxy. The housing is machined from A-40 material and is environmentally sealed with soldered-in feedthroughs, waveguide window, and an epoxy attached cover. In Figure 8 is shown a plot of the gain and noise figure for the MMIC frontend low noise amplifier.

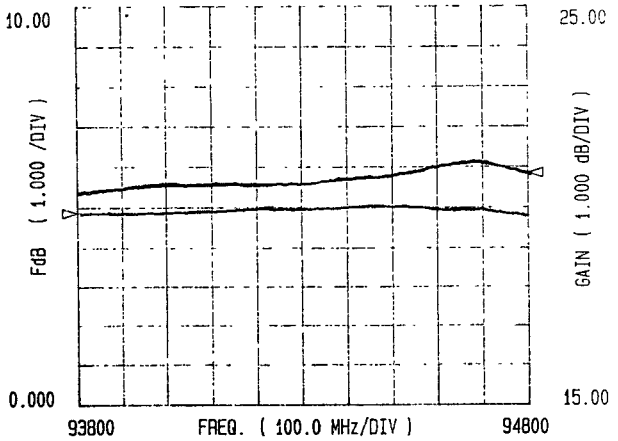


Fig. 8. Plot of noise figure and gain for the MMIC frontend low noise amplifier.

The chirped transmitted signal (94.0 to 94.5 GHz) reflected from the target is mixed with the 90 GHz DRO signal, producing the first IF, a sweep from 4.0 to 4.5 GHz.

The first IF signal is amplified, filtered, and mixed again with the sweeping YIG oscillator (4.0 to 4.5 GHz). With both RF input signals to the second mixer being the same, there should be a DC only component to the second IF output signal. However, the transmitted and reflected signal is time delayed compared to the direct connection between the YIG oscillator and the second mixer. The time delay between both chirped signals produces the frequency difference which is present at the second IF mixer output port. A frequency profile best suited to the expected range has been developed. The frequency profile requires that the chirped signal sweep from 4000 to 4500 Mhz in 2.0 msec. The time between frequency sweeps is 38 msec.

The YIG frequency sweep slope requirement is 250 MHz per msec. The dynamic tuning linearity requirement is +/- 0.3% deviation from a straight line. The transceiver preformance was conformed to be within +/-0.15%, by measurement. The YIG oscillator was selected as the swept signal source due to its exceptional frquency linearity capability. However, there are two aspects to its behavior that must be considered.1. Yig oscillators typically display hysteresis when the frequency sweep direction is reversed. 2. YIG oscillators typically display a frequency lag. The lag rate of change is dynamic in the first period from initial turn-on. The lag rate of change settles to a constant within 0.5 msec, and remains at that value for the rest of the sweep.

The first aspect of YIG behavior is not a concern to the RailSentry application. The second aspect, frequency lag, is a real phenomena which must be considered when applying a YIG oscillator to the RAilSentry application requirement of ±0.3% linear deviation. The resulting frquency profile, dictated by the YIG oscillator, is that the frequency sweep actually be swept from 3800 MHz to 4500 MHz in 2.80 msec. The first 200 MHz are swept in 0.8 msec, leaving the remaining 2.0 msec for the optimal remaining 500 MHz (from 4000 to 4500 MHz). The constant frequency lag as the YIG sweeps from 4000 to 4500 MHz is consistent with the RailSentry linear deviation requirement.

All the Transceiver requirements have been complied with, as demonstrated by field measurements and tests. The parameters and electrical performance requirements are presented in Table 2. Transmitted signal levels greater than +18 dBm could be achieved by additional power amplification. This versatility positions the Transmitter for possible use in other applications.

Parameter	Requirement	Capability
Tx Freq. Band	94-94.32 GHz	94-94.5 GHz
Tx output power level	+18 dBm	+18 dBm
Rx Freq. Band	94-94.32 GHz	94-94.5 GHz
Chirp Bandwidth	322 MHz	500 Mhz
Chirp pulsewidth	2.80 msec	2.80 msec
Chirp frequency	140 Hz	140 Hz
Rx input Signal Range	-20 to-90dBm	-20 to -130 dBm
Noise Figure	12 dB, SSB	6.17 dB, SSB*
Dynamic Range	70 dB	110 dB

* SSB (single side band)

Table 2. Radar Transceiver Requirements vs capability.

CIRCUIT DESIGNS

Some designs were based on computer simulations. Touchstone, Eagleware, SysCalc, and Spice all proved to be valuable tools. Frequency ranges, gain, noise figure, and dynamic range were all primary electrical parameters in the design.

YIG OSCILLATOR SWEEP CIRCUIT

The basic funciton of this circuit is to provide a linear voltage sweep from 0.0 Vdc + 10.0 Vdc in 2.8 msec. The DSP TTL Trigger input signal provides for the system timing of 2.80 msec of frquency sweep and 38 msec of cycle time. One of two sets of contacts of a quad FET switch are used to connect a precision voltage source to the input of an operational amplifier. The op-amp integrates and inverts the constant negative ten volt level to a linear ramp ranging from 0.0 Vdc to + 10.0 Vdc. The second set of FET switch contacts closes when the first set opens, thereby "dumping" the capacitive charge in the op-amp feedback branch. The capacitive discharge occurs in

approximately 0.5 msec, preparing the circuit for the next voltage ramp cycle. The capacitors in the op-amp feedback branch are high quality polypropylene components, selected for very low leakage current properties. The temperature variations behavior of these capacitors was also considered in their selection. The voltage ramping circuit output is connected to the YIG oscillator frquency control line (part of the voltage to current converter-Driver). The resulting voltage sweep is very linear, comparable in performance to the linearity capability of the YIG oscillator. The output voltage ramp is presented in Figure 9.

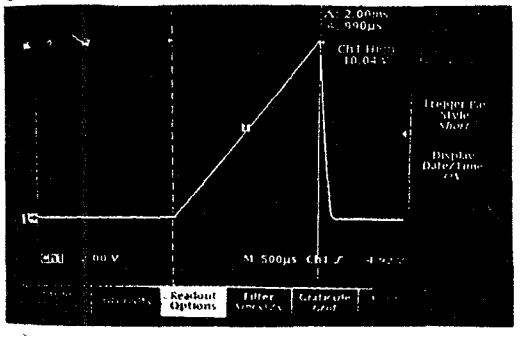


Fig.9. YIG oscillator voltage ramp circuit output waveform.

SECOND DOWNCONVERTER CIRCUIT

The second Downconverter is desgined to operate over a frquency range from -30 to -90 dBm. The equivalent output signal level is -13 to -73 dBm. Two stages of RF gain are provided by MGA-86576 low noise amplifiers. These are wideband devices, allowing for flat gain performance without the need for tuning. A bandpass filter defines the frquency range of operation. The typical Noise Figure of the MGA-86576 amplifiers is 1.6 dB at 4000 MHz. The output signal is applied to the second mixer input port. Additionally, a second similar signal is applied to the mixer LO input port. The circuit configuration includes shorted 1/4 wavelength de-coupling lines in the bias circuits at 4250 MHz. This design was examined on EAGLEWARE software, and subsequently verified by actual measurement. The measured data confirmed that the second Downconverter is linear at -40 dBm and below.

SECOND I.F. CIRCUIT

The second IF circuit consists of a highpass filter, an ultra low noise amplifier, a variable gain amplifier, and a lowpass filter. The input signal range of operation extends from -14 to -74 dBm. The output signal level is +10 dB and is kept constant by the variable gain amplifier. The two lumped element filters define the frequency band from 10 KHz to 3.30 MHz.

The preamplifier is configured around a ComLinear CLC 425 ultra low noise operational amplifier, with 1.05nV/Hz$^{1/2}$. the input impedance is 50 ohms, necessary for a good RF match with the highpass filter. The output impedance is 50 ohms so that a good match is established when looking at this stage separately (a test point is provided for this purpose). The stage gain is designed for 30 dB, but the input and output 50 ohm impedances sacrifice 6 dB, for the resulting 24 dB gain. This was anticipated.

The variable gain amplifier is configured in two stages. ComLinear CLC 522 operational amplifiers are used to achieve a dynamic range in excess of 70 dB. External buffer stages and differential pair quadrant amplifiers are not required because the CLC522 incroporates these features as internal features. The output amplifier is also included in the CLC 522. The input impedance of both stages of the variable gain amplifier is 510 ohms. This was done as a compromise with the gain-bandwidth product limitation of the CLC522. The output impedance of both stages is 50 ohms. Again, this was done to facilitate testing if individual stages are to be examined. There is a minimal interstage loss of -0.9 dB due to the impedance ratios, which is acceptable.

The output signal level of 2 Vp-p in a 50 ohms system was selected as the maximum undistorted output level. This corresponds to + 10 dBm. The gain of each variable stage is designed for 35 dB. The loop bandwidth of the variable gain stages is established by an RC time constant lowpass filter in the gain control line. The RailSentry Transceiver loop bandwidth of 10 Khz (equivalent time constant of 15.9 usec) was selected as the design goal. A five times margin was established for the variable gain amplifier. The loop bandwidth of the variable gain amplifier design goal was set at 50 KHz (corresponsding to the time constant of 3.183 usec). The second IF circuit performance is presented in Figure 10. It can be seen that the frequency response is flat form 10 KHz to 3.3 MHz. The test was conducted at several gain levels, with -13, -30, -59, and -69 dB of gain. All responses are flat in the desired frequency range.

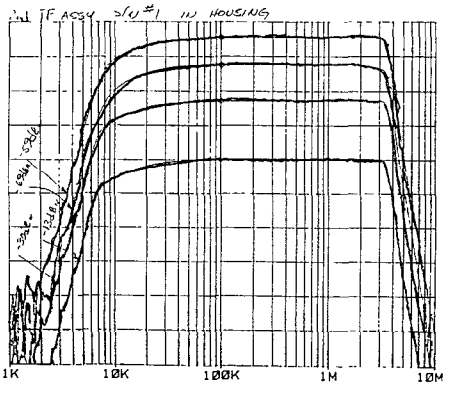


Fig. 10. Second IF output frequency responses.

CONCLUSIONS

The Radar Transceiver has been developed on a commercial contract with the Siemens Transportation Systems, Inc. as part of the P2000 contract with the Los Angeles County Metropolitan Transportation Authority. Six Technology Demonstration Models will be delivered in early 1996. To date, performance measurements have exceeded frequency range, noise figure, linearity, and dynamic range requirements.The Transceiver is a state-of-the-art development, utilizing MMIC devices at 94 GHz.